WAFER SPRAY COATING FOR PRE-APPLIED UNDERFILL

Akira Morita and James Klocke
Nordson ASYMTEK
Carlsbad, CA, USA
akira.morita@nordsonasymtek.com; james.klocke@nordsonasymtek.com

ABSTRACT

Recently, the process of pre-applying underfill onto a wafer is getting attention in 3D packaging. The pre-applied underfill material is placed on the bumped side of the wafer before dicing. Then the dies (with underfill) are stacked on another chip or wafer after dicing. There are a few ways to apply underfill onto the wafer: vacuum lamination, spin coating, and spray coating. Each of them has different challenges.

- Vacuum lamination needs expensive vacuum lamination equipment.
- Spin coating has material wastage.
- Spray coating must make consistent coating thickness over wafer.

This paper will demonstrate that using our experience with conformal coating and jet dispensing, we have evaluated wafer spray coating for pre-applied underfill application. This paper will present how we address the thickness consistency and wastage reduction challenges when using wafer spray coating.

Key words: 3D package, underfill, pre-applied, wafer coating, spray coating, material wastage.

INTRODUCTION

3D packages with through-silicon vias (TSV) have been enjoying a strong momentum recently for use in many semiconductor applications such as memory, MPU, application processor, and FPGA in mobile, data center and telecom applications. This is because these semiconductors need more bandwidth, and have a smaller form factor that saves power for the end applications.

Underfill for 3D packages includes two types: underfill between stacked silicon dies for micro-bump bonding, and underfill between silicon die and organic substrate for conventional flip chip bonding. Both types of underfill are usually required for a 3D package. The same technologies such as capillary underfill for a single flip chip package are applicable to the underfill between silicon die and organic substrate. The underfill between stacked dies needs a new technology in terms of both material and application methods mainly because of the tight geometries, even though there is no CTE mismatch between stacked silicon dies.

In 3D packaging, very tight bump pitch and bump height between stacked dies are required, for example, 25um bump height and 40um pitch. This geometry makes the conventional underfill process (capillary underfill) difficult in terms of underfill penetration speed under dies and increases the possibility of undesirable void creation.

There are three major technologies to apply underfill: capillary underfill, molded underfill and pre-applied underfill. Capillary underfill has been the dominant technology since flip chip technology began. Molded underfill has emerged recently for high-volume production especially for mobile devices because it combines the two processes of over-molding and underfill. Because capillary and molded underfill techniques apply underfill after die bonding, they are significantly challenged by the tight bump pitch and height between stacked dies because of slow penetration speed (even no penetration) and void possibility.

On the other hand, pre-applied underfill is not challenged by tight bump pitch/height because it is applied before die bonding. Therefore, pre-applied underfill is getting attention in the market. Pre-applied underfill on a wafer is especially attractive because bumps on die don't have to go through an underfill layer to reach the pads. In underfill on backside of the dies (non-bumped side), bumps on dies have to go through the underfill. And application on wafer is more productive than application on chip by chip.

REQUIREMENTS FOR PRE-APPLIED UNDERFILL

For a long time, pre-applied underfill has been used for flip chip packaging as long as the die size is small (such as less than 5mm) and the bump number is fewer than ten. These conditions can avoid pre-applied underfill challenges relatively easily: trapping fillers between bumps and pads, and trapping air in the underfill (voids) during the bonding process. But many existing and potential 3D package devices such as FPGA, MPU, memory and application processors have larger die size and significantly more bumps (i.e. >10,000 bumps) compared to the traditional devices adopting pre-applied underfill.

Underfill material suppliers suggest many various formulas and bonding/curing processes including temperature profiles and pressure for preventing the two challenges.

Additionally, underfill coating shape on wafer such as thickness, topology and tolerance have been defined gradually with coordination between underfill material formulators and equipment manufacturers. Typical shape requirements include the following.

- Flat underfill surface
- Bump tops appear on underfill surface
- Thickness +/-10% tolerance
  (Typical thickness is 20um ~ 40um)

Figure 1 shows three shapes of underfill. Underfill height 2 is the most popular requirement currently. Underfill height 1 could be acceptable because of other process and material conditions. But Underfill height 3, which has hollow surfaces between bumps, is unacceptable because the hollow surfaces trap air in bonding.

The underfill thickness is mainly determined by the underfill volume requirement between dies. If the pad side surface on another die (counter part of die with underfill) is irregular because of circuitry, the required volume would change.

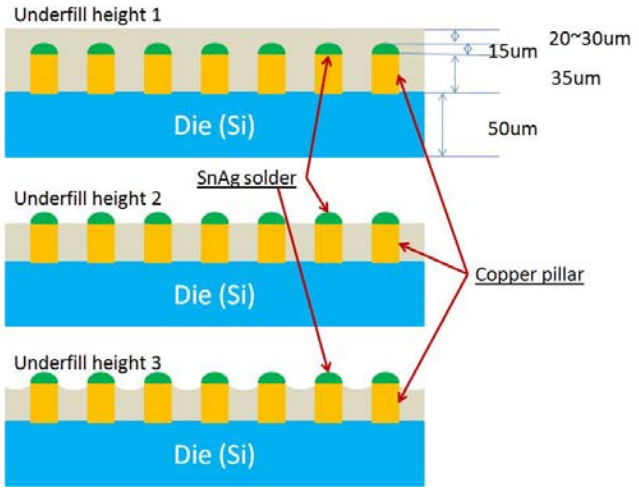

Figure 1. Pre-applied underfill shapes with different volume

These shape requirements are important to consider when selecting an underfill application technology.

APPLYING PRE-APPLIED UNDERFILL
Vacuum lamination, spin coating, and spray coating are processes used to apply uniform thin films or coating to flat substrates.

Vacuum lamination
Vacuum lamination has several different processes by equipment suppliers. The following process [1] is an example and Figure 2 illustrates the process flow below.

1. The substrate and film base pre-applied underfill or non-conductive film (NCF) are loaded into diaphragm vacuum chamber.
2. Vacuuming starts from substrate side and pressurization starts from NCF side.
3. Diaphragm makes NCF stick to substrate by pressure, and heat is applied to substrate if necessary.
4. Vacuuming and pressurization are reversed to release and unload the substrate.

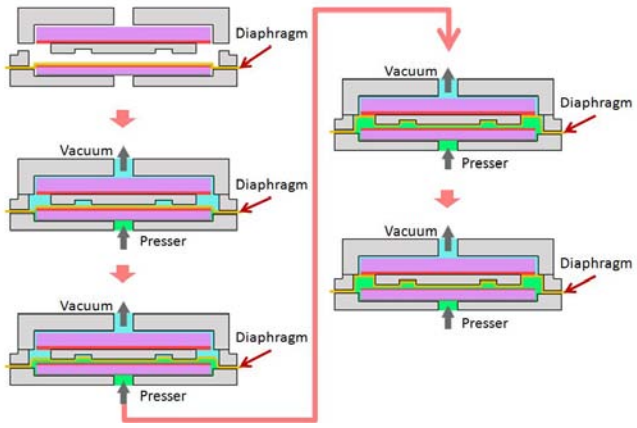

Figure 2. Vacuum lamination process flow chart

Spin coating
Spin coating has been established as described below, and is illustrated in Figure 3.

1. The substrate is loaded on a rotator.
2. An excess amount of a solution is placed on the substrate, which is then rotated at high speed in order to spread the fluid by centrifugal force.
3. Rotation continues while the fluid spins off the edges of the substrate, until the desired thickness of the film is achieved.

Figure 3. Spin-coating process flow chart [2]

Spray coating
Spray coating has several different processes. The following process was used for this study, and its flow chart is in Figure 4 below.

1. The substrate is loaded into a spray coating machine.
2. The spray applicator starts coating the substrate while the system coordinates fluid flow rate, substrate rotation rate and coating thickness.
3. The substrate is unloaded after coating is complete.

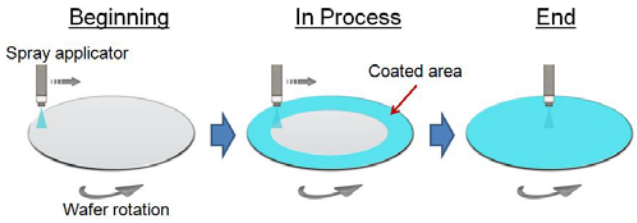

Figure 4. Spray coating process flow chart

Pre-applied underfill by spray coating is shown in Figure 5.

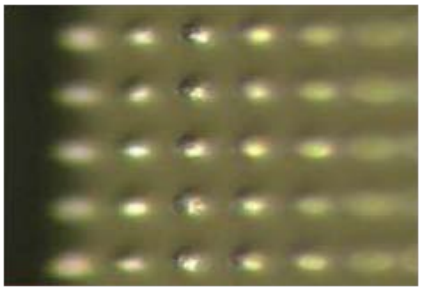

Figure 5. Pre-applied underfill by spray coating

APPLYING PROCESS PROS AND CONS

Vacuum lamination pros and cons

The process of vacuum lamination has been applied to various film applications such as die attach film and back grinding tape. It has advantages such as thickness uniformity and flatness after lamination. These advantages are valuable benefits for pre-applied underfill requirements. On the other hand, bumps need to go through non-conductive film (NCF) so that bump tops appear on the NCF surface. As a result, the underfill surfaces between bumps have s creases or deformation. The deformation can be flattened by heat and/or an adjustment to the viscosity of the underfill used in the vacuum lamination process. Another way to prevent the deformation is to make holes on the NCF, matched with bump locations on the wafer in advance. In this case, the vacuum lamination machine needs to make the alignment between bumped wafer and NCF for the holes to match. [3]

This process needs pressure to make NCF stick to the bumped wafer. This pressure could break interconnection layers (BEOL) if the layers are low-k material. Vacuum lamination is suitable to the entire wafer. It is difficult to laminate NCF on just specific areas on wafer. Under certain conditions, such as 2.5D applications where the wafer is used as a silicone interposer, only selective areas need pre-applied underfill. In this application, pre-applied underfill is required on the wafer interposer and not on the die. Thus, there are areas on the interposer that do not require underfill and must be selectively removed. Vacuum lamination has limitations for this request.

Vacuum lamination needs relatively expensive equipment, more than $250,000, because it requires vacuum chamber and hole alignment. And equipment size also is larger than others: more than 3m wide.

Spin coating pros and cons

Spin coating has been used for many years to apply thin layers of photoresist to semiconductor wafers. This is a highly reliable and well-studied method of applying coatings. With adjustments to the fluid viscosity and control of the spin speed, a recipe can be developed to predict the coating thickness. More complicated recipes can be developed with multiple spin speeds to overcome problems with single-speed coating. In some cases spin coaters can be housed inside sealed chambers to control the evaporation rate of solvents in the coating materials, allowing better coverage of non-flat topographical features, such as walls and edges on MEMS devices.

Spin coaters use a variety of spray heads to apply photoresist and other materials to wafers. Fan- and cone-shaped sprays are often used to dispense an even coating on the wafer. In addition, ultrasonic spray heads have been employed to create a mist over the wafers. However they almost always use low-viscosity fluids and the speed of the wafer spinner to control the coating thickness on the wafer.

One major disadvantage to spin coating of wafers is the amount of wasted material. Coating material is flooded onto the center of the wafer, and it is thrown laterally at high speed to obtain a desired thickness. With 200mm diameter wafers it is estimated that approximately 48% of the materials applied to the wafer ends up wasted (as it spins off the wafer). With larger, 300mm wafers the waste is in the 75% range. This is one of the reasons that ultrasonic misting heads are used in spin coaters, to minimize wasted fluid. Although ultrasonic heads produce fine spray mists with a tight distribution of particles in the range of 25um, they need low-viscosity materials to function effectively. When using inexpensive fluids, the waste is not so much of a problem, but when materials cost over $1000 per liter, it becomes very expensive to coat wafers with poor transfer efficiencies.

Other problems that result from the spin process, such as edge beads, can cause downstream problems. The bead is a product of the spinning of the fluid and surface tension effects at the edge of a wafer. Equipment manufactures add separate spray attachments to the wafer spinners to remove the edge beads, using a small spray of solvent. This adds complexity and cost to the process, and a solvent/resist waste stream. One good feature of spin coating is its ability to coat over minor surface problems cause by dried water spots. The shearing action can actually move particles or other forms of contamination. However coatings may pull back if there is an area on the wafer where the fluid does not wet to or a small pit or projection (from the surface) exists.

Because spin coating needs low-viscosity fluids, it is not uncommon for users to thin high-viscosity fluids with solvent and apply several coatings on a wafer to get to a desired thickness. Dilution of materials can limit the fluid formulator's options. There are some cases when the

material formulators would prefer to use high-molecular-weight adhesives, which have higher bond strength. If the material is thinned with solvent, the adhesive strength is lowered. With adhesive thickness on the order of 10um there is very little adhesive to start with, and to lower the adhesive strength to facilitate the coating equipment is not desirable.

Spray coating pros and cons

Spray coating is quite popular and used in many various industries. In the electronics industry, conformal coating on printed circuit board assemblies (PCBA) by spray applicator with silicone, urethane and other materials has been established for higher reliability electronics, protecting moisture from penetrating the PCBA. Also, flux coating is a major spray coating application for flip chip packaging and CSP/BGA assembly on board.

Spray technology intrinsically gives atomized liquid direction: thus selective coating (coating selective areas of a substrate) is possible. The edge definition of selective coating varies, depending on spray applicator technologies and liquid materials. Tight edge-definition ranges could be a few millimeters, which is the distance between no-coating area edge and coating area edge with pre-determined coating thickness. Therefore, a spray applicator can coat just the wafer area without much wastage. This is a clear advantage over spin-coating for pre-applied underfill. And this selective coating could be used to coat a specific area on a wafer, while spin-coating and vacuum lamination are limited in selectivity.

Spray applicators can adjust atomizing parameters such as fluid pressure and nozzle size to accommodate a wide range of fluid viscosities to make consistent coating. This is another advantage over spin-coating, which has just rotation speed for its major adjustment. And higher viscosity range is also another challenge. The rotation/spray process has been reported by several authors [4] but not using high-viscosity fluids.

However, thinner coating thickness and consistency of thickness are major challenges for spray coating against pre-applied underfill requirements because typical thickness and consistency requirements are 20um ~ 30um +/- 10%.

By reducing to a fairly low rotation speed, such as less than 1000 rpm, any edge build up, which happens in spin-coating, would be eliminated as well as any shadowing effect if you have a bump structure on the wafer. An atomizing spray head is used to create adhesive particles from the highly viscous fluid. This process does not flood the wafer, or use the spin/shear effect to thin the fluid layer. To coat the wafer a controlled arc motion path for the spray head is used. This results in an even coating over a 300mm diameter wafer, to within a few microns uniformity. Coverage is uniform to the edge of a wafer within 1mm of edge. See Figure 4 for a process flow for spray coating.

This study focuses on the following points to evaluate the technical feasibility of wafer spray coating equipment.

- Coating thickness on wafer: 20um
- Coating consistency: +/-10%
- Material wastage: less than 20%

APPARATUS FOR ROTATION/SPRAY PROCESS

Spray coating equipment for this study includes:

- An X-Y robotic dispenser system
- An air atomizing spray applicator
- Speed-programmable wafer rotator
- An integrated balance scale

The coating set-up for rotation/spray process consists of a speed-programmable wafer rotator and chuck. These are situated inside the X-Y robotic dispenser that is using the spray applicator. The air spray applicator uses a cone-in-seat valve adjustment system to vary the fluid flow. Typical application settings are;

- Fluid pressures range 2 to 3 PSI (0.14 to 0.21 bar) to >30 PSI (>2 bar)
- Atomization pressures range 10 to 50 PSI (0.69 to 3.4 bar)
- Nozzle diameter range 0.003 to 0.010 in. (0.0075 to 0.025 mm).

The rate of fluid flow is controlled by using a patented mass flow controller device that is integrated into this system. Through testing, the mass flow characteristics of the applicator can be determined by setting a flow rate from the applicator and characterizing this with a film thickness. Figure 6 shows the mass flow calibration principle.

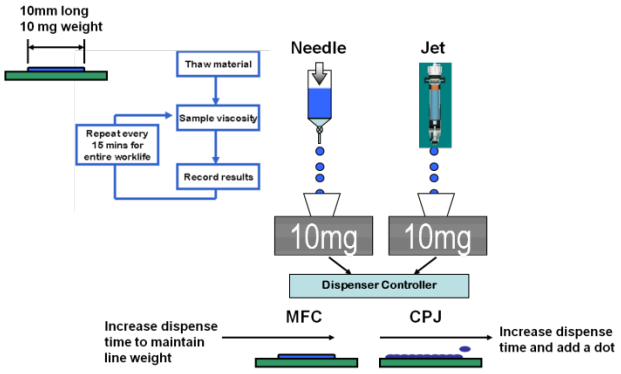

Figure 6 Mass Flow Calibration principle

A particular issue with rotation/spray to consider is that the linear speed of a spinning wafer at the circumference is large and zero at the center. Therefore the control of the spray applicator movement has to compensate for this problem. At the same time, if uniform coating to the edge of the wafer is critical, the spray applicator has to be able to coat to the very edge of the wafer, with minimal waste of fluid at the edge. Figure 7 shows a 300mm wafer that has been coated using this process.

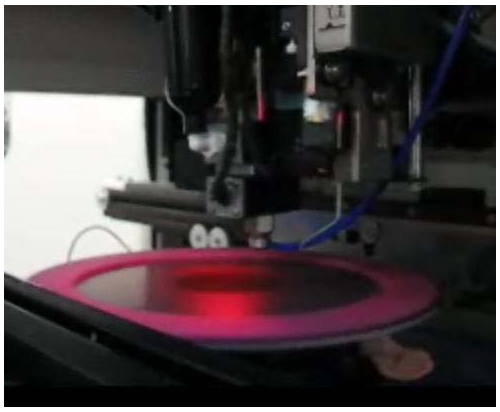

Figure 7. 300mm wafer that has been coated

COATING THICKNESS MEASUREMENT METHOD

Coating thickness is measured by profilometer. For accuracy, the bare wafer surface was revealed by scratching off the coated area. Then a profilometer measured the distance between coated area and bare wafer area, see Figure 8.Measurement results by profilometer for 20um thickness are shown Figure 9.

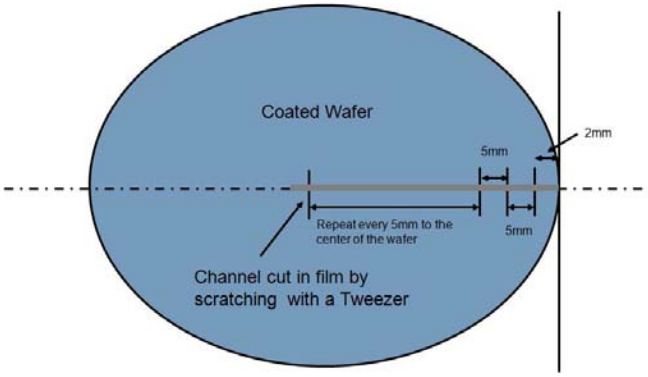

Figure8. Coating thickness measurement method diagram

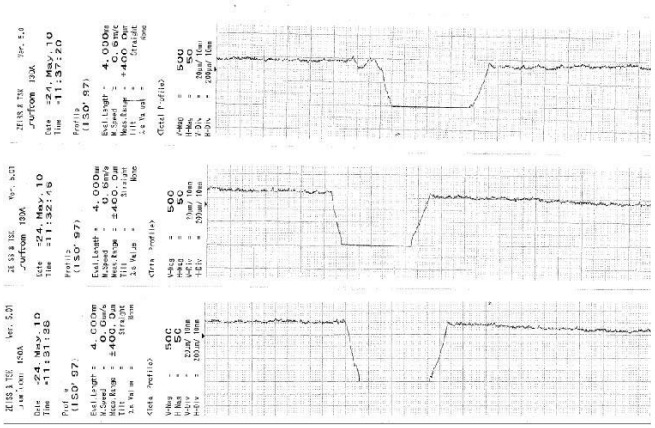

Figure 9. Measurement results by profilometer for 20um thickness

RESULTS

With a 300-mm diameter wafer, the volume of fluid on the wafer was typically 1 gram of material. Several different spray applicator motions were evaluated but the preferred motion was an arch across the wafer. Depending on the film thickness accuracy required, the coating time for a 300mm wafer was as low as 13 seconds. But if an accuracy of +/-10% was required on a 20um thick film, the coating time was as long as 120 seconds.

Spray coating thickness was measured for a wafer using a 20um thickness target. The thickness distribution (Figure10) shows the coating consistency is within 20um +/-10%. Coating coverage is uniform to the edge of a wafer within 1mm of edge.

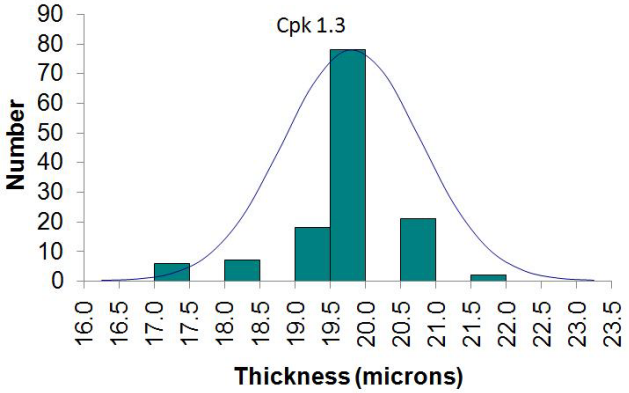

Figure 10. Spray coating thickness distribution for wafers.

Material wastage was measured for 4 wafer samples; results are shown in Table 1. All of the samples show less than 20% of material wastage.

Table 1. Material wastage results

Sample #	Blank Wafer wt. [gm]	Dis. Wafer wt. [gm]	Initial Syringe Wt. [gm]	After dis. Syringe wt. [gm]	Wafer net dis wt. [gm]	Syringe net dis. wt. [gm]	Wastage [gm]	Wastage [%]	Dist. From edge [mm]
1	52.7174	53.5882	36.0588		0.8708	1.0641	0.1932	18.2	0
2	51.2733	52.1463			0.8730	1.0641	0.1911	18.0	0
3	51.5687	52.4431			0.8744	1.0641	0.1897	17.8	0
4	51.6906	52.5685		31.8026	0.8780	1.0641	0.1861	17.5	0

Material wastage was measured by comparison between syringe weight change and wafer weight change before and after coating.

CONCLUSIONS

3D package requirements dictate the need for thin and consistent coating of pre-applied underfill materials. Pre-applied underfill volumes require 20um ~ 30um film thicknesses, with a +/-10% tolerance (on the thickness). Material wastage should be minimized to save costs. The process must be flexible (high volume/low mix and low volume/high mix) with regard to selectively placing the underfill material only where it is needed, and the coating process equipment should be minimally invasive (small footprint) to the production floor.

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REFERENCES

1. Company website for MEIKI, http://www.meiki-ss.co.jp/mac/index.html.
2. Spin-coating entry for Wikipedia-Netherlands http://nl.wikipedia.org/wiki/Bestand:SolGel_SpinCoating.jpg
3. Eric Huenger, et al., “Development of a Low Temperature Curing Aqueous Base Developable Photoimageable Dielectric for Wafer Level Packaging,” IMAPS Device Packaging, March 2012.
4. Mark Whitmore, Jeff Schake, “Screen and Stencil Printing for Wafer Backside Coating,” 33rd International Electronics Manufacturing Technology Conference, 2008.